THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SCOTT C. PETLER

Appeal No. 1997-4115
Application No. 08/325,765[1]

ON BRIEF

Before KRASS, MARTIN, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1, 2, 4-10, and 12. The appellant filed an amendment after final rejection on November 26, 1996, which was entered. We reverse.

[1] The application was filed on October 19, 1994.

BACKGROUND

The invention at issue in this appeal generates logic for an output encoded finite state machine (FSM). A conventional FSM typically employs delay (D) flip-flops to store an encoded value that indicates the current state of the FSM. An output decoder generates outputs of the FSM based on the current state as determined from the value stored by the D flip-flops.

An FSM that uses output flip-flops, i.e., flip-flops placed at the outputs of the FSM, to encode states of the FSM is called “an output encoded FSM.” The output encoded FSM works correctly when each state has a unique combination of output values. When more than one state has the same combination of output values, however, the output flip-flops cannot uniquely identify each state. Additional flip-flops must be added to the output encoded FSM to allow the unique identification of each state. By taking advantage of unspecified output values, i.e., "don't care" values, the invention reduces the number of flip-flops that need to be added.

The invention receives an output encoded FSM from a user. The output encoded FSM specifies states, transition conditions between the states, and output values for each state. At least one output value is unspecified for at least one state, i.e., the user indicates that the output value is a don't care.

Based on the output encoded FSM, the invention generates logic. For each output of the FSM, an output flip-flop that stores the output values is generated. Values are assigned to unspecified output values. The assigned values are selected so that each state can be uniquely identified by current values stored by the output flip-flops and a minimum number of additional flip-flops. The assignment is done by determining a number of times that output values between two states are identical for every combination of values for the unspecified output values. The combination of values which results in the fewest number of times output values between two states are identical is the combination of values assigned to the unspecified output values.

Claim 1, which is representative for our purposes, follows:

> 1. A method for generating logic for a finite state machine, the method comprising the steps of:
>
> (a) receiving, from a user, input which specifies states of the finite state machine, transition conditions between states and output values for each state, wherein at least one output value is unspecified for at least one state; and,
>
> (b) generating logic for a finite state machine from the inputs received in step (a) including, for each output of the finite state machine, generating an output flip-flop which stores the output, the generating of the logic including the following substep
>
> (b.1) assigning values to unspecified output values so that each state can be uniquely identified by current values stored by the output flip-flops and a minimum of additional flip-flops.

The references relied on in rejecting the claims follow:

Washabaugh	5,452,215	Sep. 19, 1995 (filed Aug. 24, 1994)
Chandra et al. (Chandra)	5,517,432	May 14, 1996. (filed Jan. 31, 1994)

Claims 1, 2, 4-10, and 12 stand rejected under 35 U.S.C. § 103 as obvious over Chandra in view of Washabaugh. Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the brief and answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. Furthermore, we duly considered the arguments of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 1, 2, 4-10, and 12. Accordingly, we reverse.

We begin by noting three principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). (1) In rejecting claims under 35 U.S.C. § 103, the patent examiner bears the initial burden of establishing a prima facie case of obviousness. (2) A prima facie case is established when teachings from the prior art would appear to have suggested

the claimed subject matter to a person of ordinary skill in the art. (3) If the examiner fails to establish a prima facie case, his obviousness rejection will be reversed. With these in mind, we analyze the appellant's arguments.

The appellant argues, "*Chandra* gives no information about how flip-flops are used or could be used within any finite state machine. *Chandra* does not even mention the term 'flip-flop'." (Appeal Br. at 8.) He adds, "*Washabaugh* does not disclose or suggest the use of flip-flops to store outputs of a finite state machine, but rather, specifically teaches the use of separate storage elements to store the state of the finite state machine. See Figure 3 and column 4, lines 17 through 18." (Id. at 9.)

The examiner replies, "Washabaugh does teach the implementation of flip flops as claimed." (Examiner's Answer at 10.) He adds, "applicants are [sic] suggested to look closely to the language of columns 5 (line 51) - column 7 (line 22) of the Washabaugh reference in which state

assignment is disclosed." (Id. at 11.) We agree with the appellant.

Claims 1, 2, and 4-7 each specifies in pertinent part the following limitations: "for each output of the finite state machine, generating an output flip-flop which stores the output" and "assigning values to unspecified output values so that each state can be uniquely identified by current values stored by the output flip-flops and a minimum of additional flip-flops." Similarly, claims 8-10 and 12 each specify in pertinent part the following limitations: "for each output of the finite state machine, generating an output flip-flop which stores the output" and "assigning values to unspecified output values so that each state can be uniquely identified by current values stored by the output flip-flops generated ... and a minimum of additional flip-flops."

The examiner fails to show a teaching or suggestion of these limitations in the prior art. Regarding Chandra, the examiner admits, "flip-flops are not explicitly referred to," (Examiner's Answer at 10), but alleges, "flip-flops are

encompassed under the logic circuits discussed." (Id.) He "points to Column 3 (line 3) - column 4 (line 56)," (id.), of the reference to support his allegation.

"A rejection based on section 103 clearly must rest on a factual basis ...." In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967). "The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not ... resort to speculation, unfounded assumptions[,] or hindsight reconstruction to supply deficiencies in its factual basis." Id., 154 USPQ at 178. Here, the cited passage is ambiguous at best. By itself, the passage possibly could be interpreted as implying the generation of some type of flip-flop. The examiner shows no basis, however, for interpreting the passage as teaching the generation, for each output of an FSM, of an output flip-flop that stores the output. Such an interpretation amounts to speculation or an unfounded assumption. We also note the examiner's admission that "Chandra did not explicitly give details about including, within the compilation means, assigning means for assigning values to unspecified output values so that each state can be

uniquely identified by current values stored by the output flip-flops and a minimum of additional flip-flops."
(Examiner's Answer at 4.)

Washabaugh does not cure these deficiencies. Figure 3 of the reference shows an FSM that is "separated into combinational and sequential portions." Col. 3, ll. 42-44. The FSM uses a "set of flip-flops 304, 306 ... 310 [that] is used to store the state information." Col. 4, ll. 17-18. Washabaugh's flip-flops 304, 306 ... 310, however, are not output-flip-flops.

More specifically, the flip-flops 304, 306 ... 310 are not placed at the outputs of the FSM to encode the state of the FSM. Instead, the flip-flops 304, 306 ... 310, merely store an encoded value that indicates the current state of the FSM. See col. 4, ll. 35-36. Figure 3 also shows that a combinational network 302 generates the outputs of the FSM based on the current state as determined from the encoded values stored by the flip-flops 304, 306 ... 310. Because neither Chandra nor Washabaugh even teaches the use of output

flip-flops, we are not persuaded that the combination of the references teaches or would have suggested "for each output of the finite state machine, generating an output flip-flop which stores the output" and "assigning values to unspecified output values so that each state can be uniquely identified by current values stored by the output flip-flops and a minimum of additional flip-flops" as specified in claims 1, 2, and 4-7 or "for each output of the finite state machine, generating an output flip-flop which stores the output" and "assigning values to unspecified output values so that each state can be uniquely identified by current values stored by the output flip-flops generated ... and a minimum of additional flip-flops" as specified in claims 8-10 and 12.

For the foregoing reasons, the examiner has not established a prima facie case of obviousness. Therefore, we reverse the rejection of claims 1, 2, 4-10, and 12 under 35 U.S.C. § 103.

CONCLUSION

To summarize, the examiner's rejection of claims 1, 2, 4-10, and 12 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
JOHN C. MARTIN Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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RECORDS MANAGER
LEGAL DEPARTMENT 20B0
HEWLETT-PACKARD COMPANY
P. O. BOX 10301
PALO ALTO, CA 94303-0890